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Impact of Logic and Circuit Implementation on Full Adder Performance in 50-NM Technologies

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Abstract: **This work presents the design and characterization of 6 full adder circuits in a 50-nm technology. This Based on the logic function realized, the adders have been characterized for performance area and power consumption. The impact of sum and carry propagation delays on the performance, power of these systems have been evaluated. The study of the above work has been carried using Micro wind 3.1 CAD tool with detailed transistor level simulations in a 50-nm technology process.**

Keywords: **Full adders, Power Delay, Power Dissipation, area.**

I. INTRODUCTION

In this work, we present an exploratory study of popular adder structures implemented in the 50-nm process and analyzed for performance, power and area. The adders selected for this study includes the 28 transistor standard CMOS full adder, mirror adder, transmission gate-based adder ,full adder 14T, 10T final full adder ,10T full adder and .Each of the adders is also classified according to the logic function realized. Using this approach, we have presented an analysis of the possible impact of logic function choice and not just circuit choice on the performance of the final adder. The study presented here is intended to highlight the implications of using a particular full adder logic function, circuit topology, and interfacing style before choosing one for arithmetic system implementation.

II. CIRCUIT TECHNIQUES

A. The 28 transistor standard CMOS full adder

B. Mirror Full Adder

C. TG Full Adder

D. Full adder 14T

E. 10T Final Full Adder

F. 10T Full Adder

The performance of a full adder circuit depends to a great extent on the type of design style used for implementation as well as the logic function realized using the particular design style. For instance, a standard CMOS implementation allows circuits to achieve a reasonable power delay product (PDP) and area with high noise margins, regular layout and relatively higher tolerance to process variations. Dynamic implementations on the other hand may yield an extremely fast design but end up paying higher costs in the overall power consumption.

Table 1: Truth Table Of Full Adder

A	B	C_{in}	Sum	C_{out}
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

A. The 28 transistor Standard CMOS Full Adder

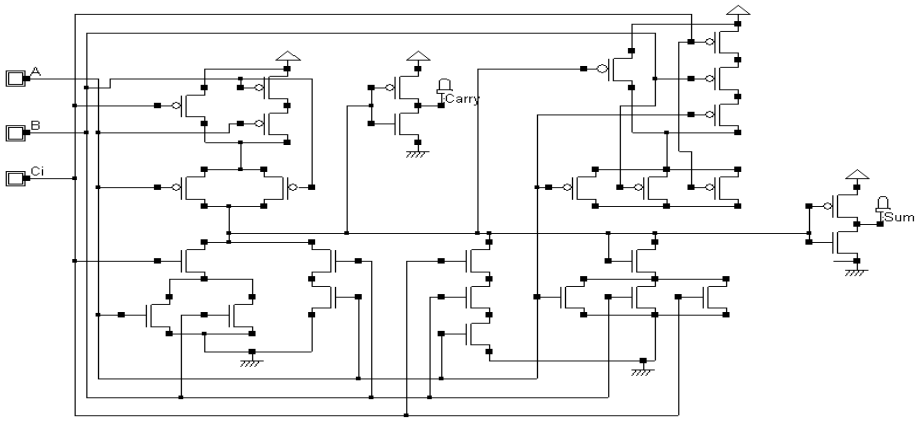

Figure A: Static Adder CMOS Adder

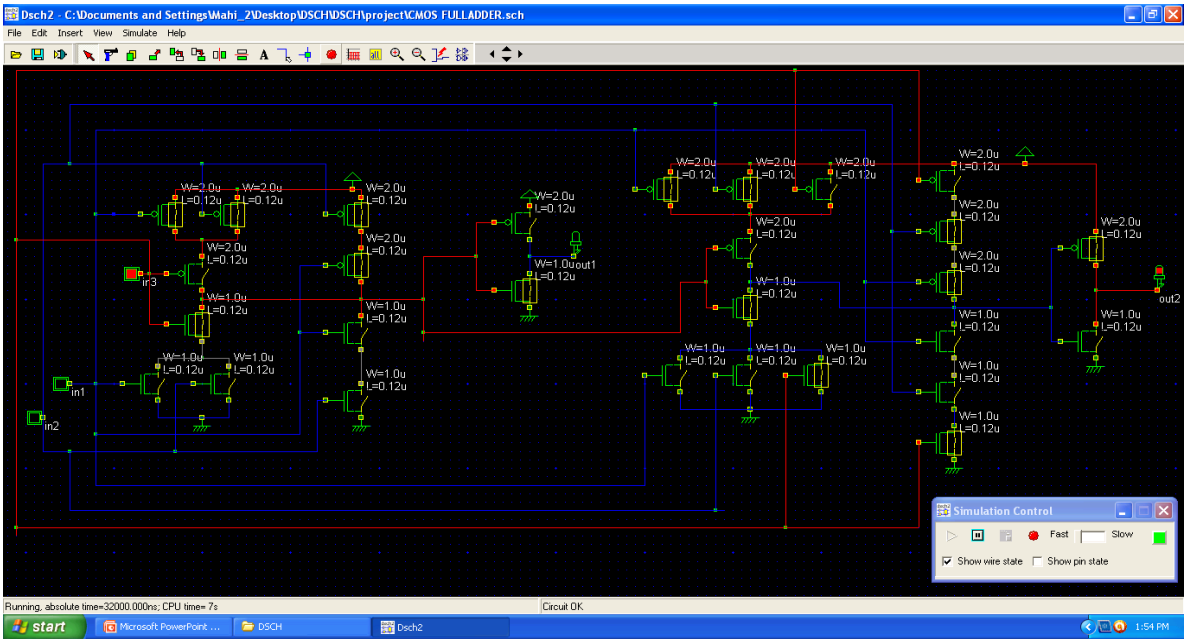

Fig A.1 DSCH DIAGRAME

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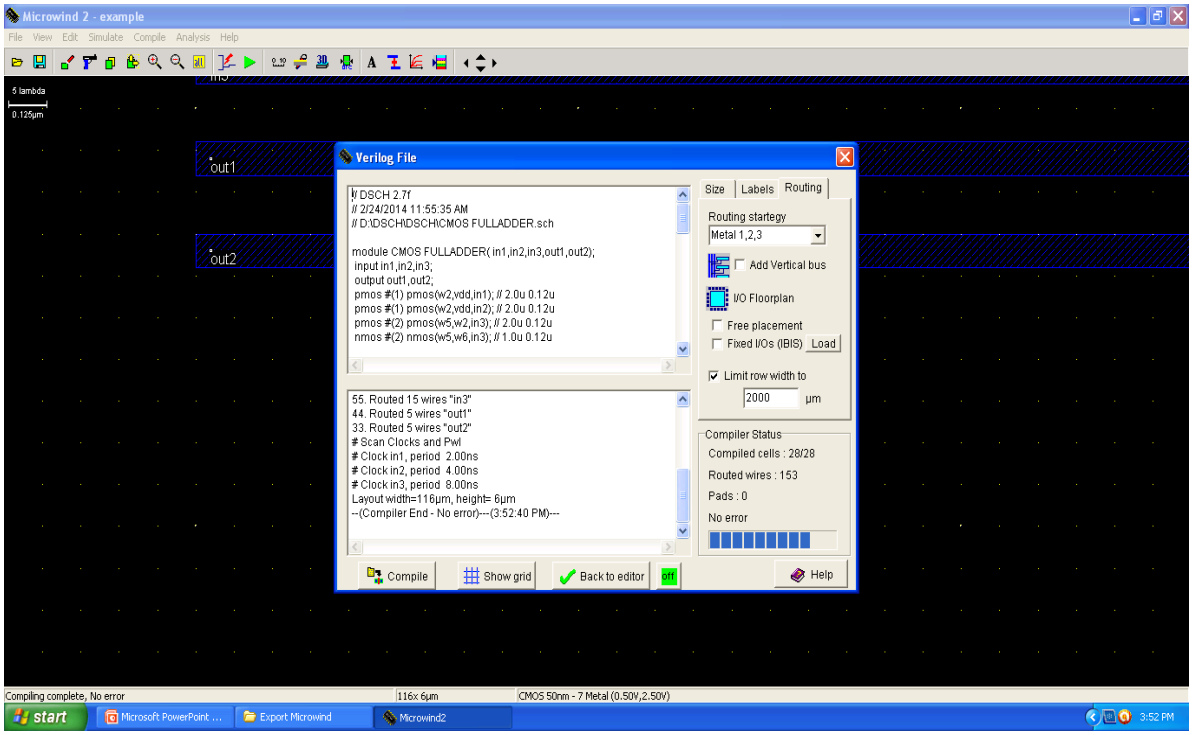
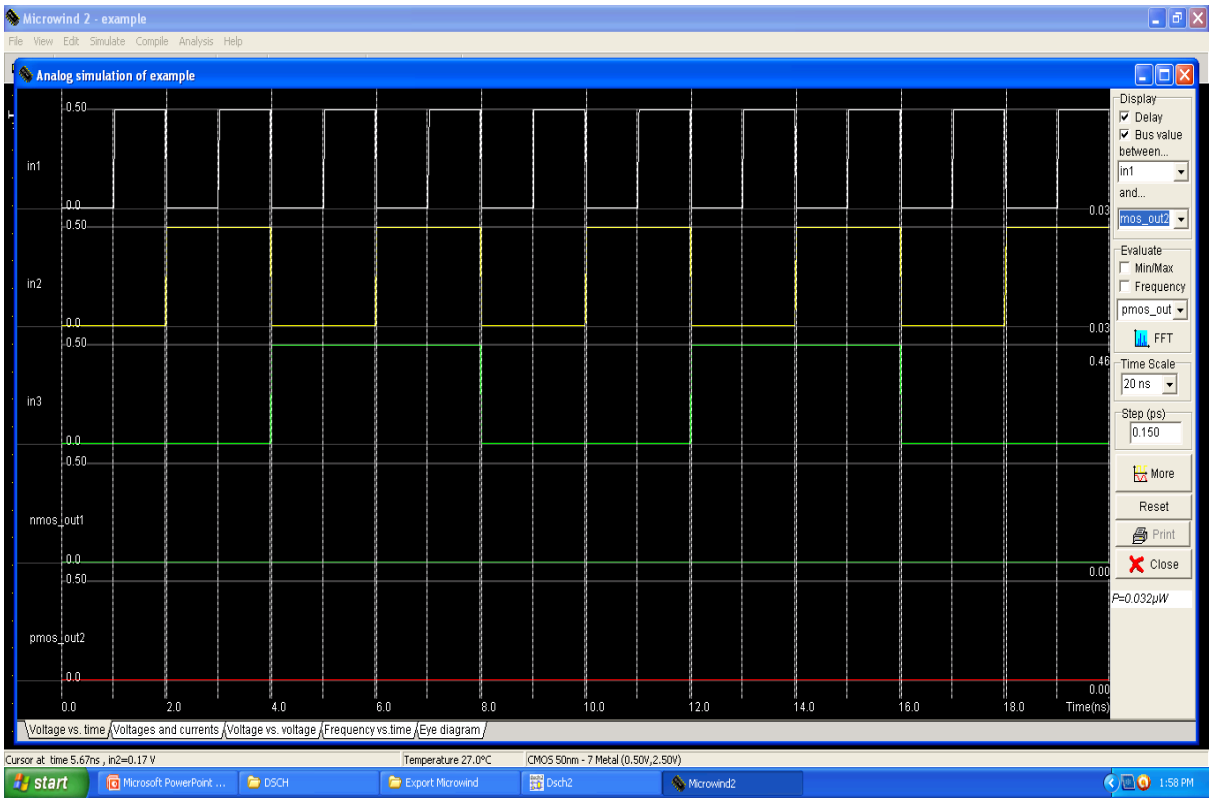




The above shown fig A is Conventional COMS full adder is a combination of PMOS pull up transistor and NMOS pull down transistor. It is well known for its robustness and scalability at low supply voltages. But its power consumption and transistor count are relatively high for low power arithmetic circuits. In this full adder, Interdependence between signals generation (SUM signal relies on the generation of COUT signal) causes the problem of delay in balance. The transmission function full adder, which uses 28 transistors for the realization of the full adder logic, of Full Adder This design uses pull up and pull-down logic as well as complementary pass logic to drive the load.

It has many advantages like low transistor count, low loading effect, better balancing between the signals than conventional full adder and it also exhibits high driving capabilities. It is in 50 nm technology the power consumption is 0.032µW and area (116*6)µm .

B. Mirror Full Adder

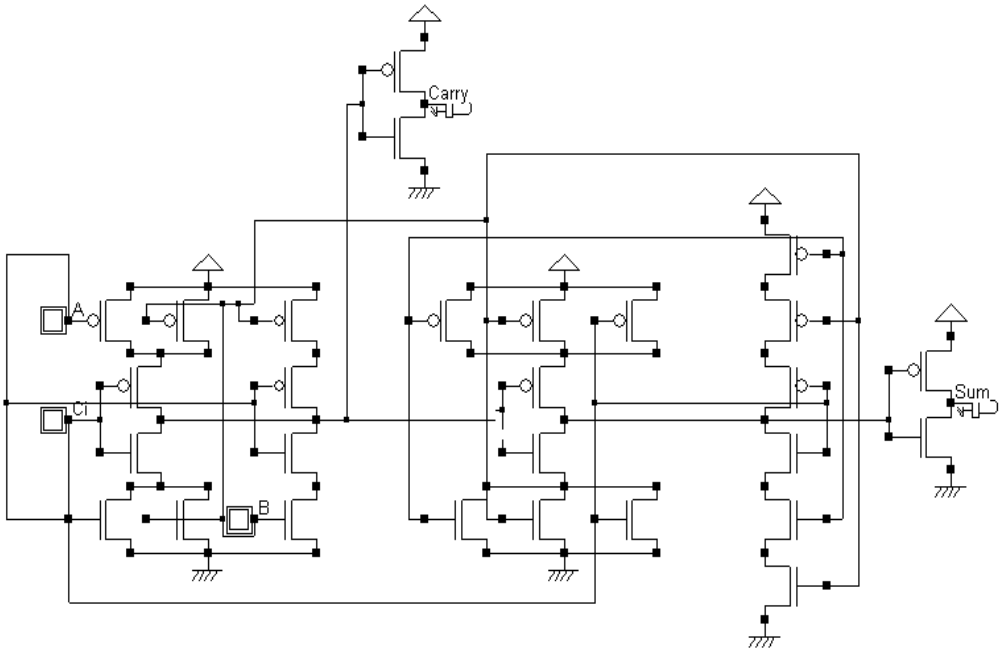
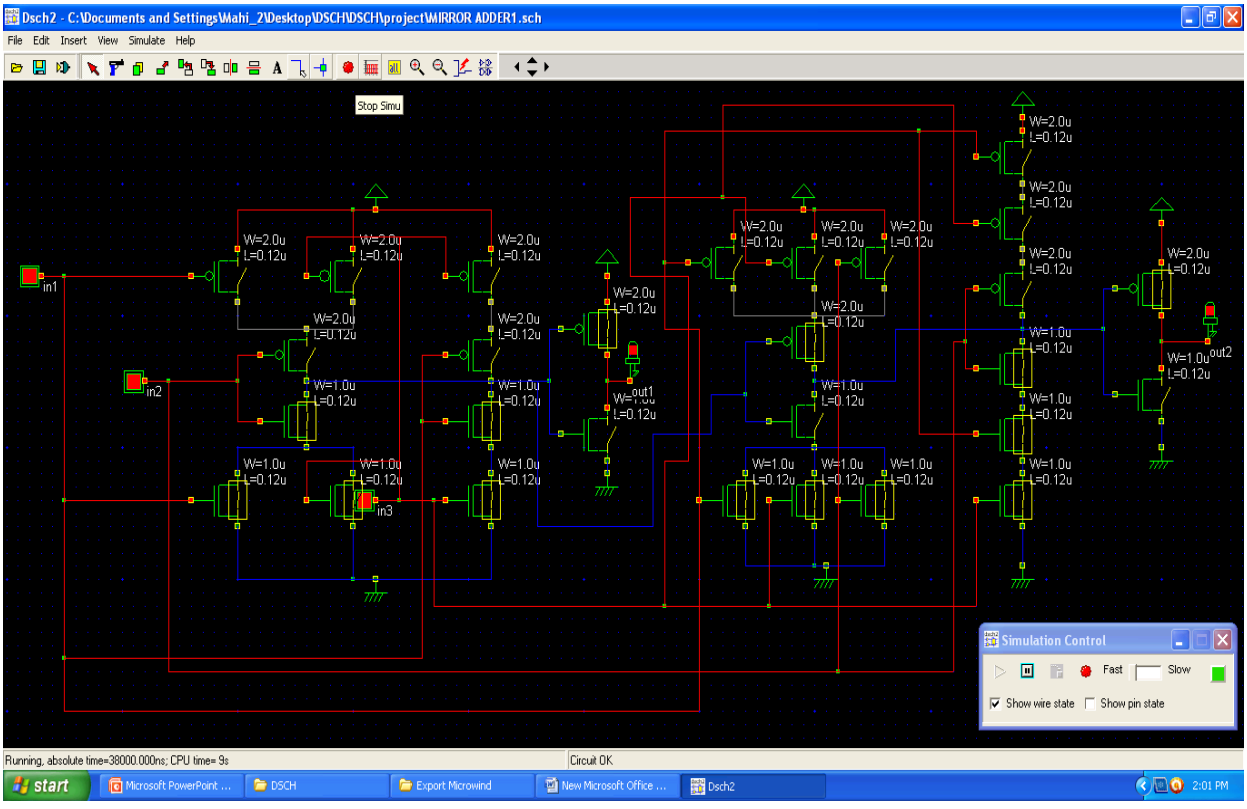


Figure B: Mirror Full Adder

DSCH DIAGRAME



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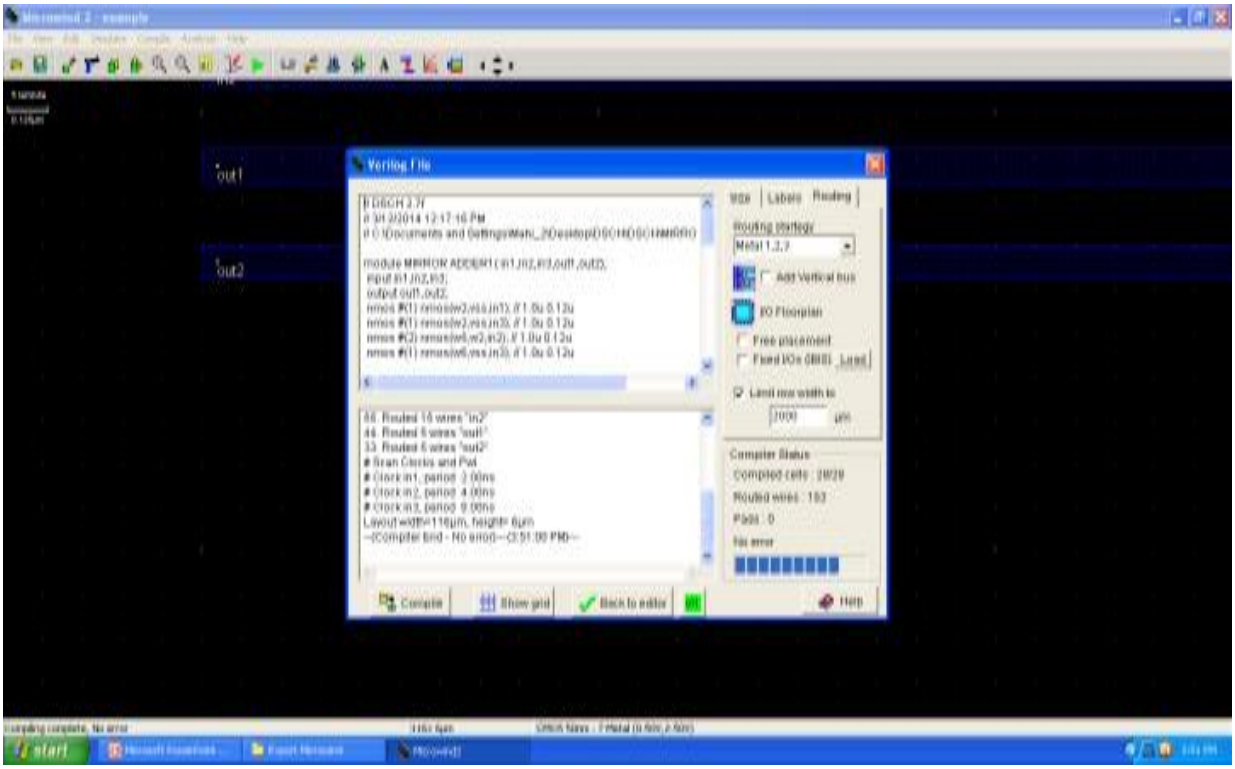
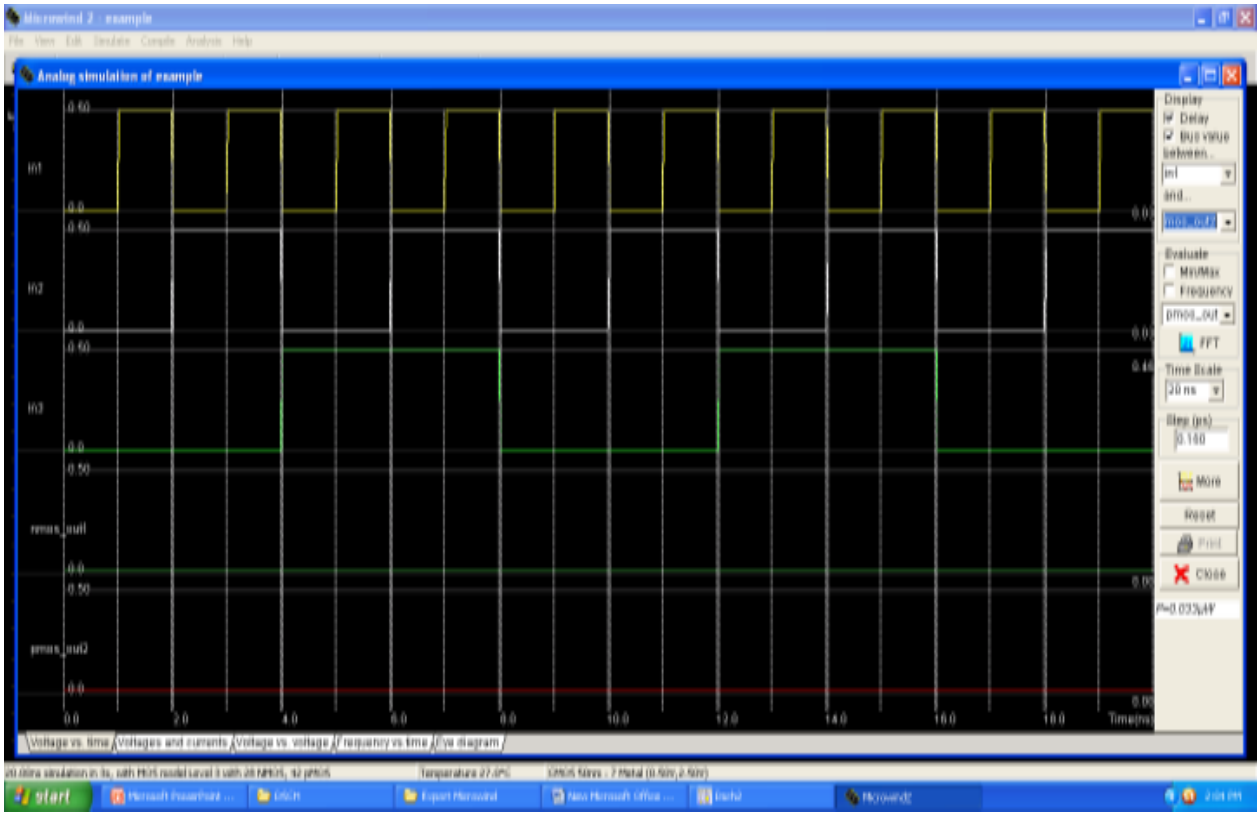
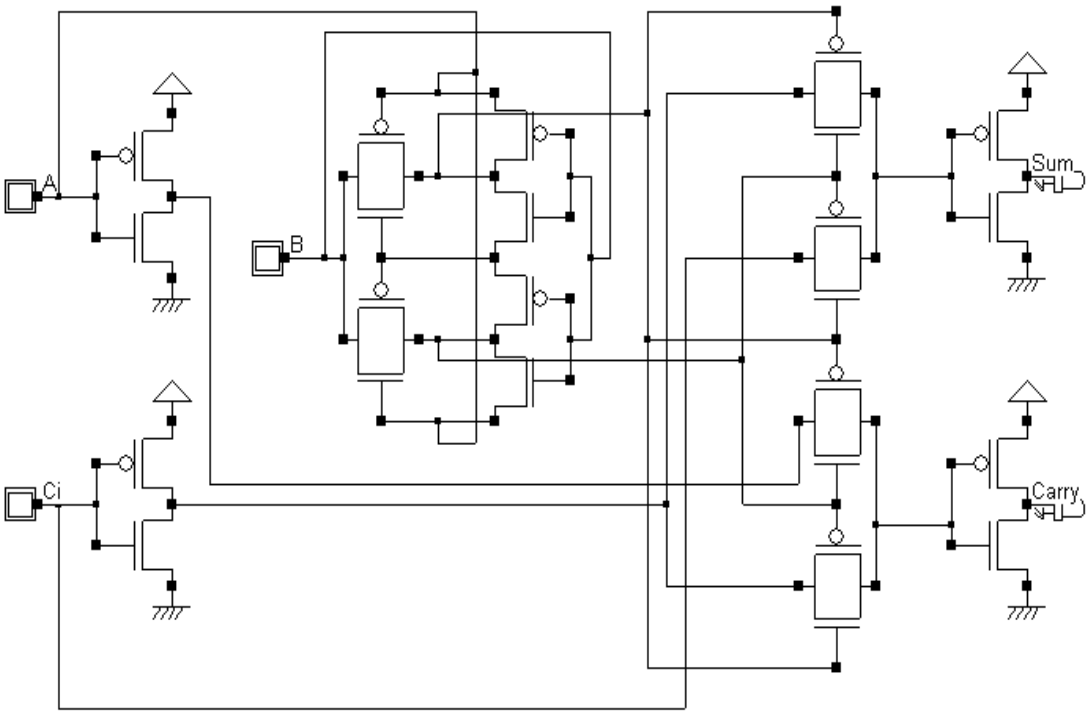




The above fig B is represented to the block diagram of the mirror adder is one of the coms full adder .it consists of 26 transistors of N-type and P-type transistors, the main purpose of the mirror full adder is to calculate the power consumption and area is better then the standard COMS full adder. Its practically the mirror adder of power consumption is 0.033µW and area (116*6) µm.

C. TG Full Adder



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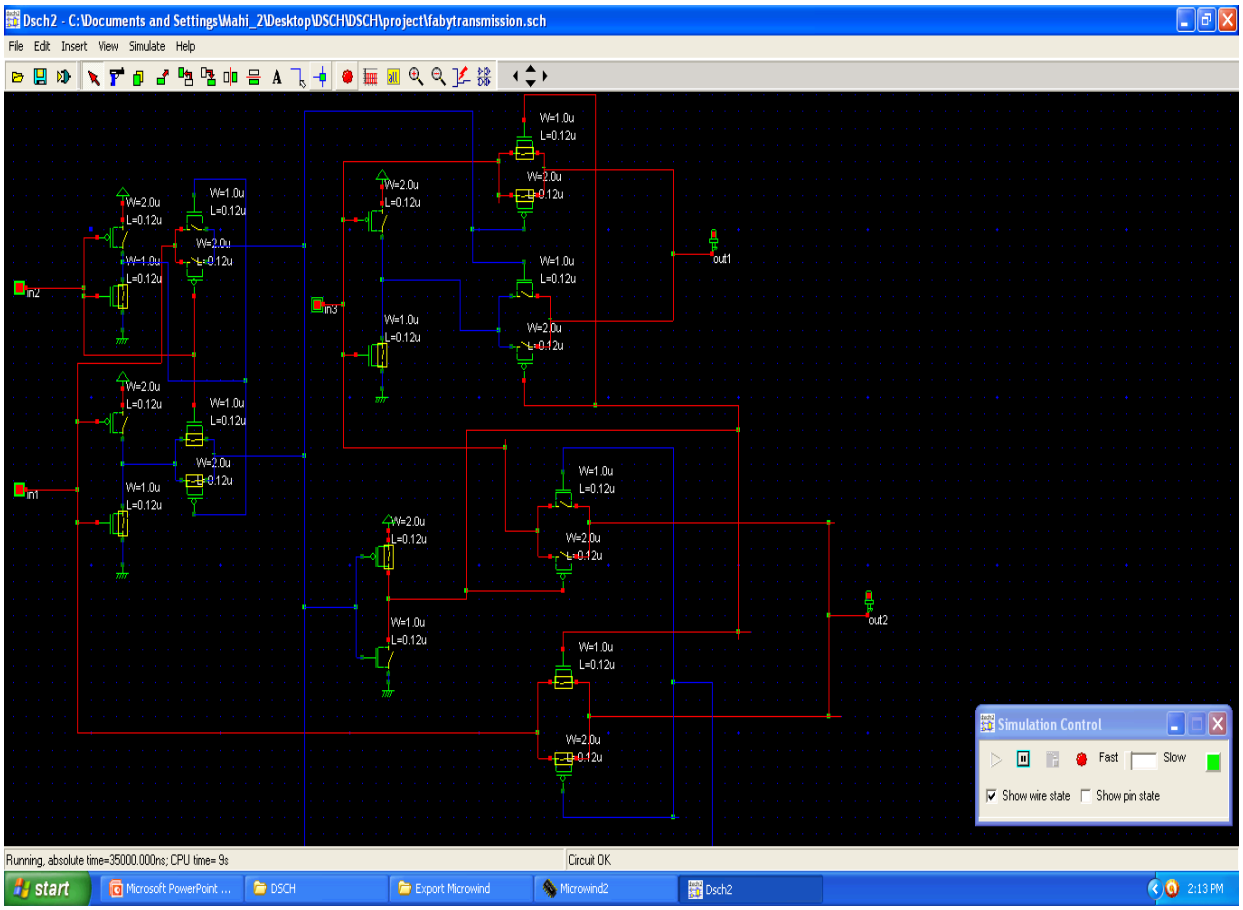

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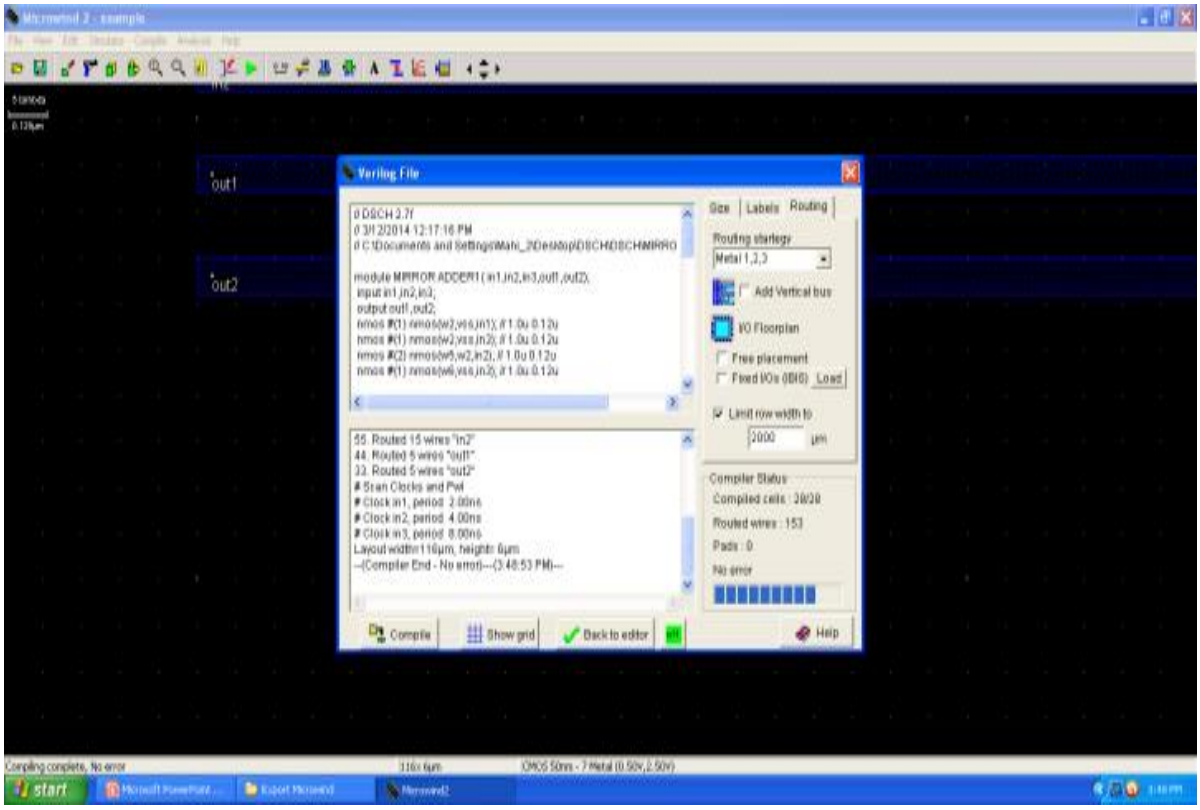
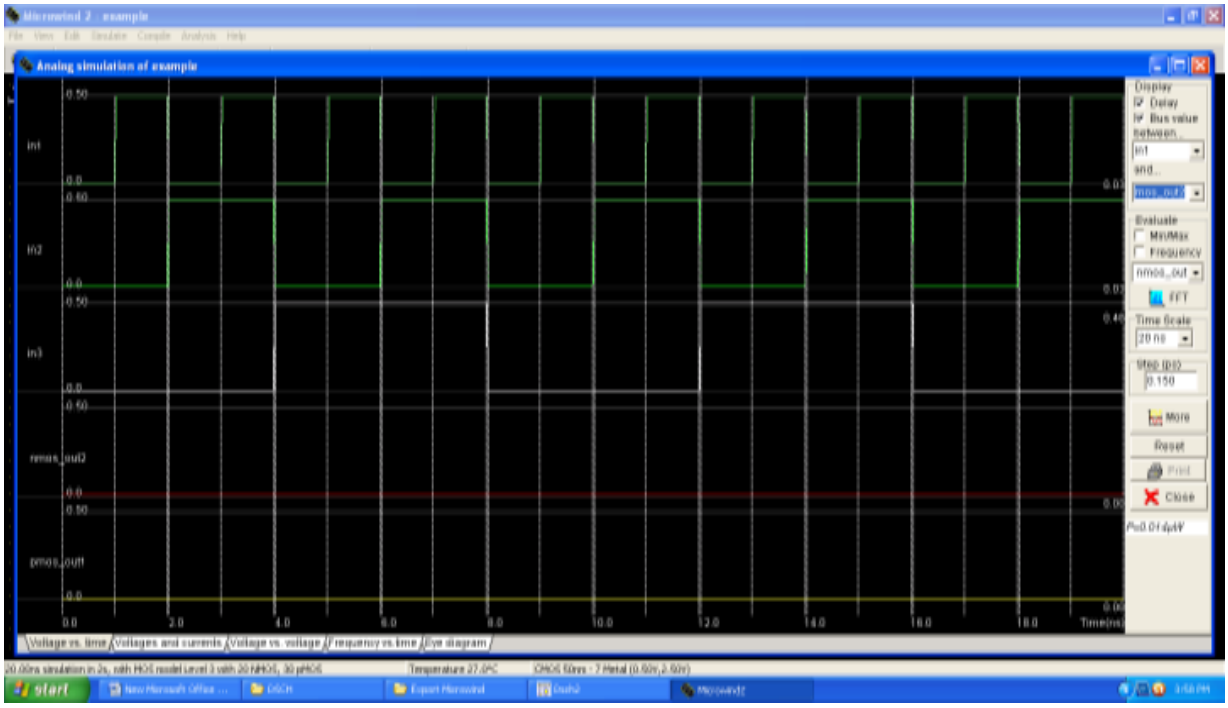
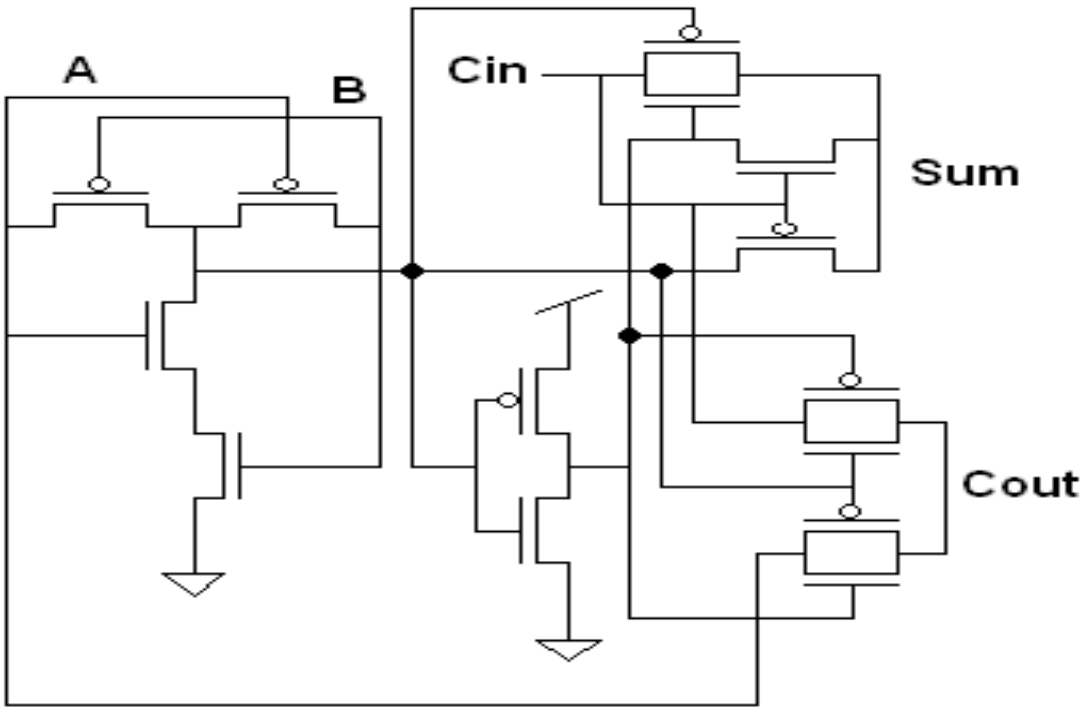




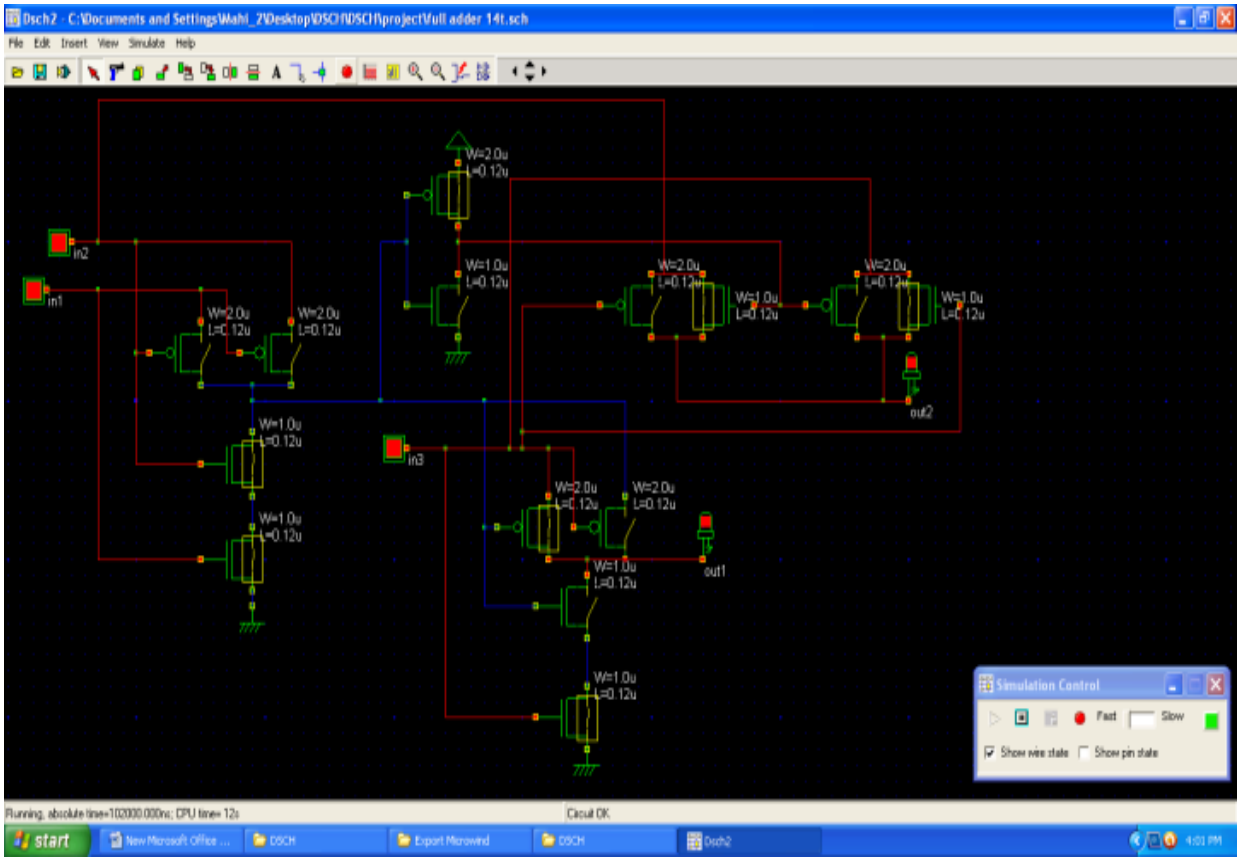
The transmission function full adder, which uses 16 transistors for the realization of the full adder logic, is shown in Fig C. This design uses pull up and pull-down logic as well as complementary pass logic to drive the load.

It has many advantages like low transistor count, low loading effect, better balancing between the signals than conventional full adder and it also exhibits high driving capabilities. Out put of the TG full adder is power consuming is 0.014µW and area is(83*6)µm

D. Full adder 14T



DSCH DIAGRAME



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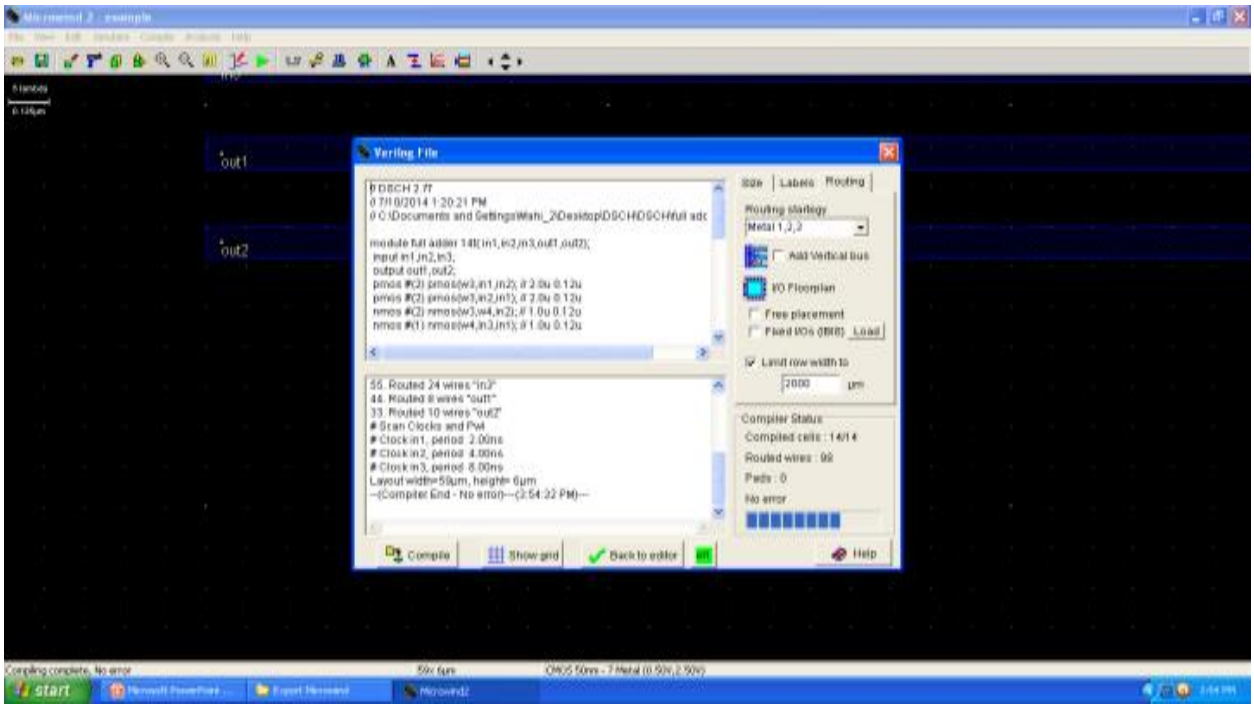
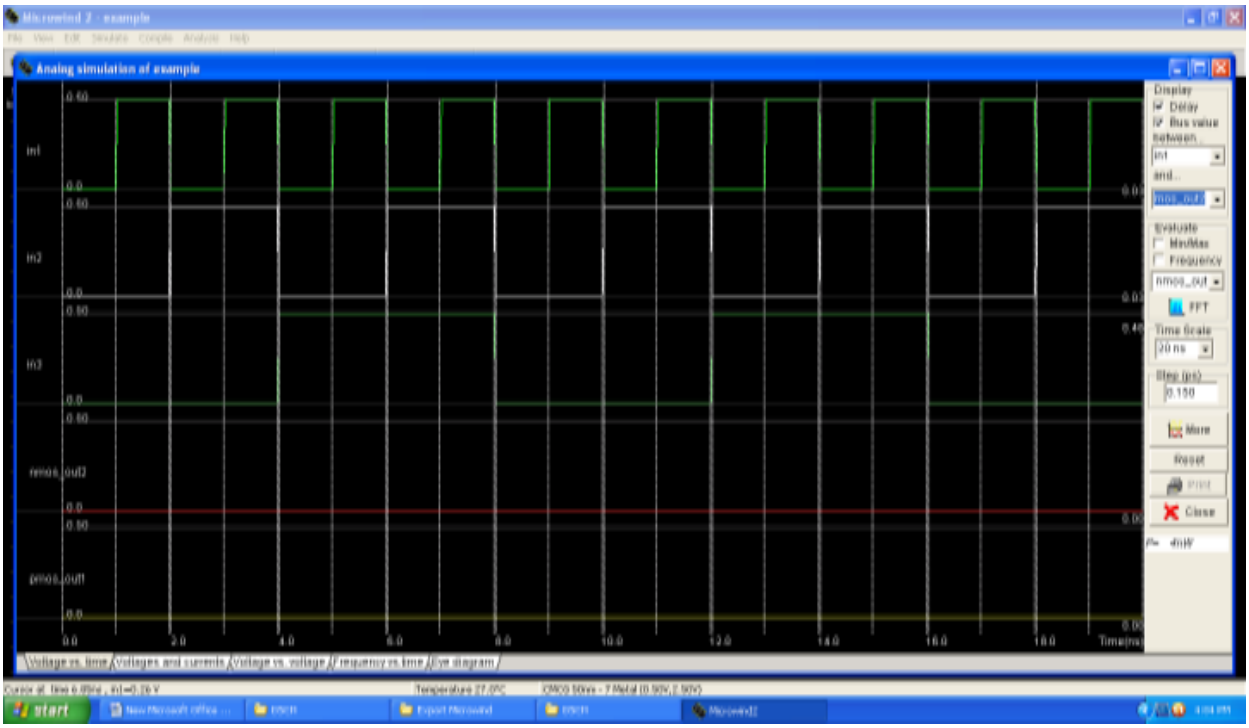


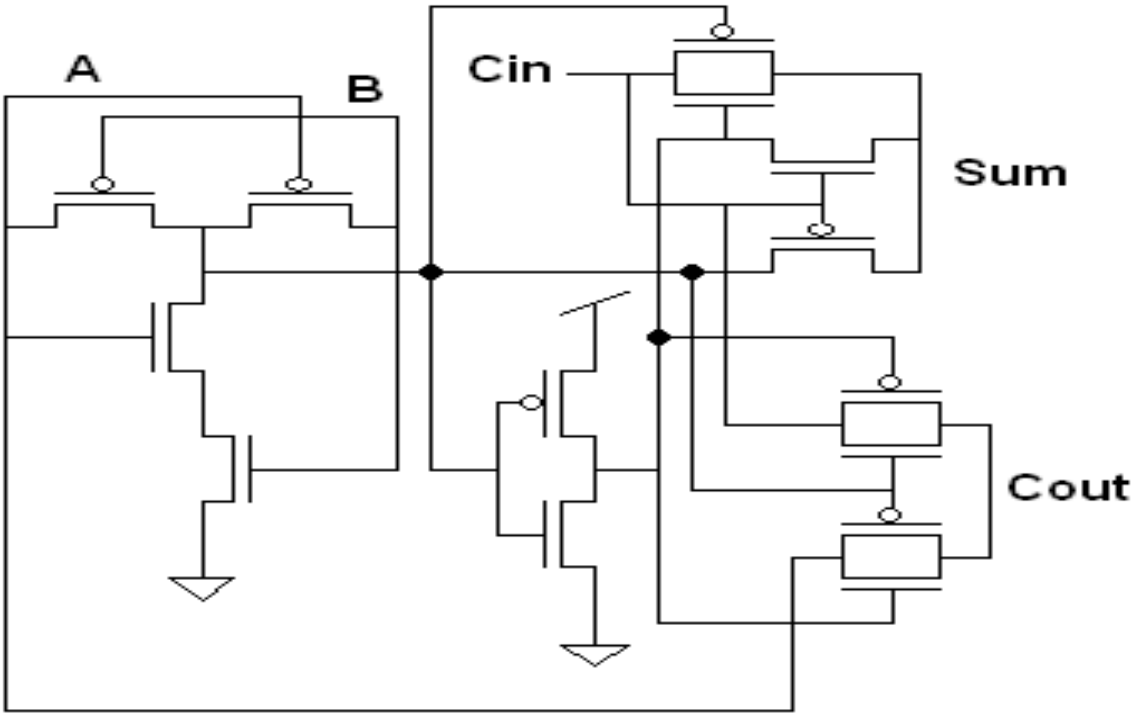


The 14T full adder contains a 4T PTL XOR gate, shown in Fig. D, an inverter and two transmission gates based multiplexer designs for sum and Carry signals.

Working principle This circuit has 4 transistors XOR which in the next stage is inverted to produce XNOR. These XOR and XNOR are used simultaneously to generate sum and cout. The signals cin and c_{in} ' are multiplexed which can controlled either by (a b) or (a ⊗ b). Similarly the C_{out} and be calculated by multiplexing a and C_{in} controlled by (a b).

Out put of the full adder power consumption is 4nW and area is (59*6)µm .Advantage of the fastest adder so far been reported. The circuit is simpler than the conventional adder.

E. 10T Final Full Adder



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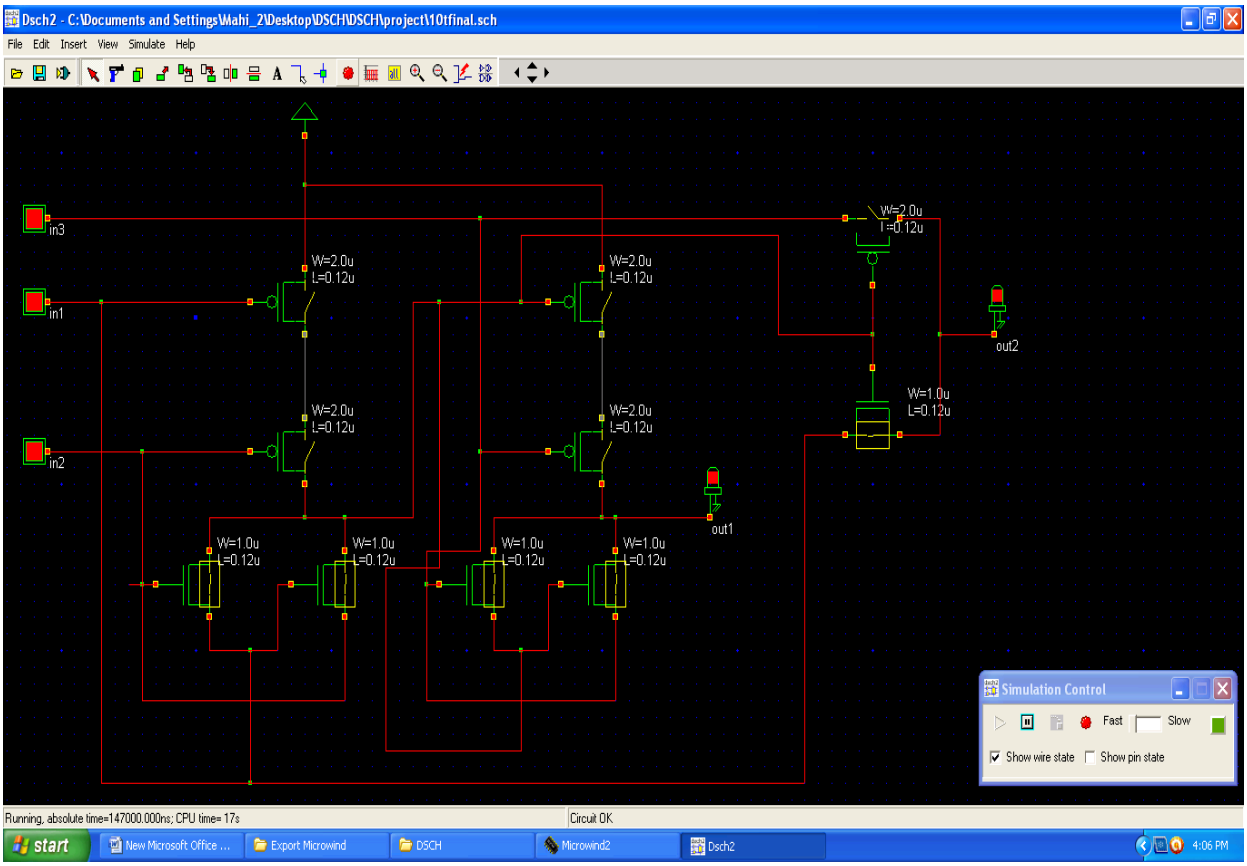

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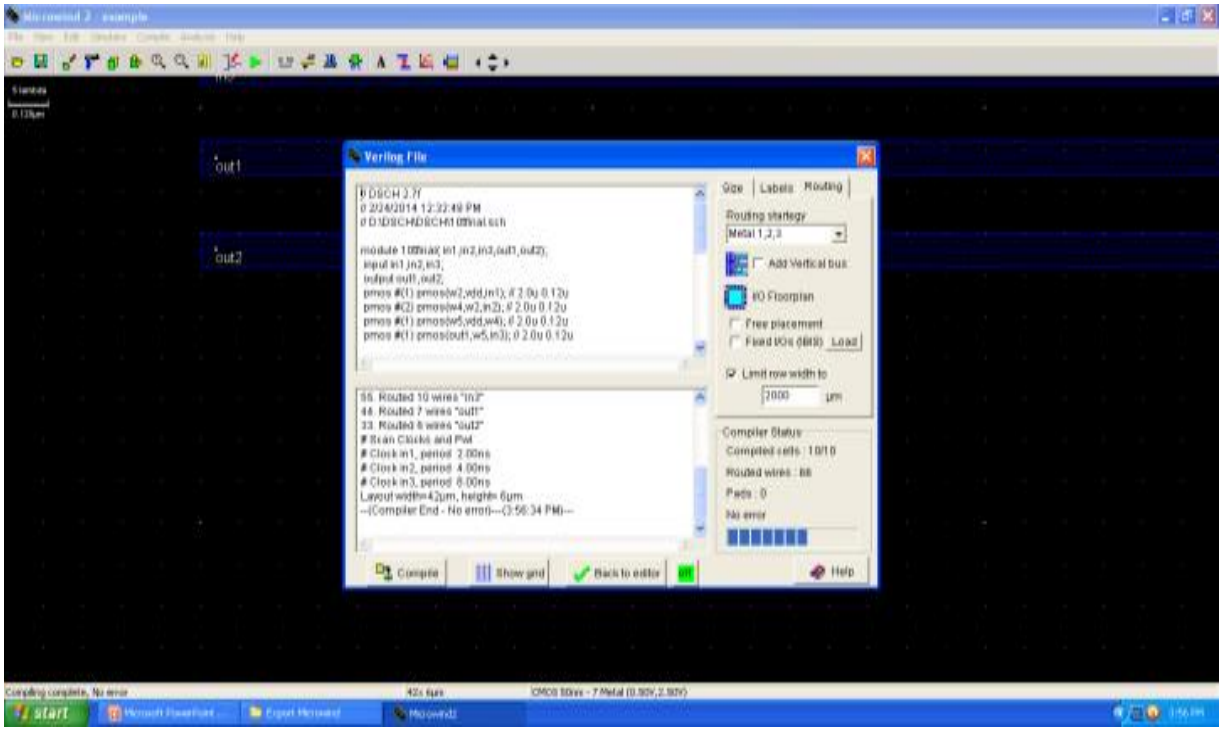
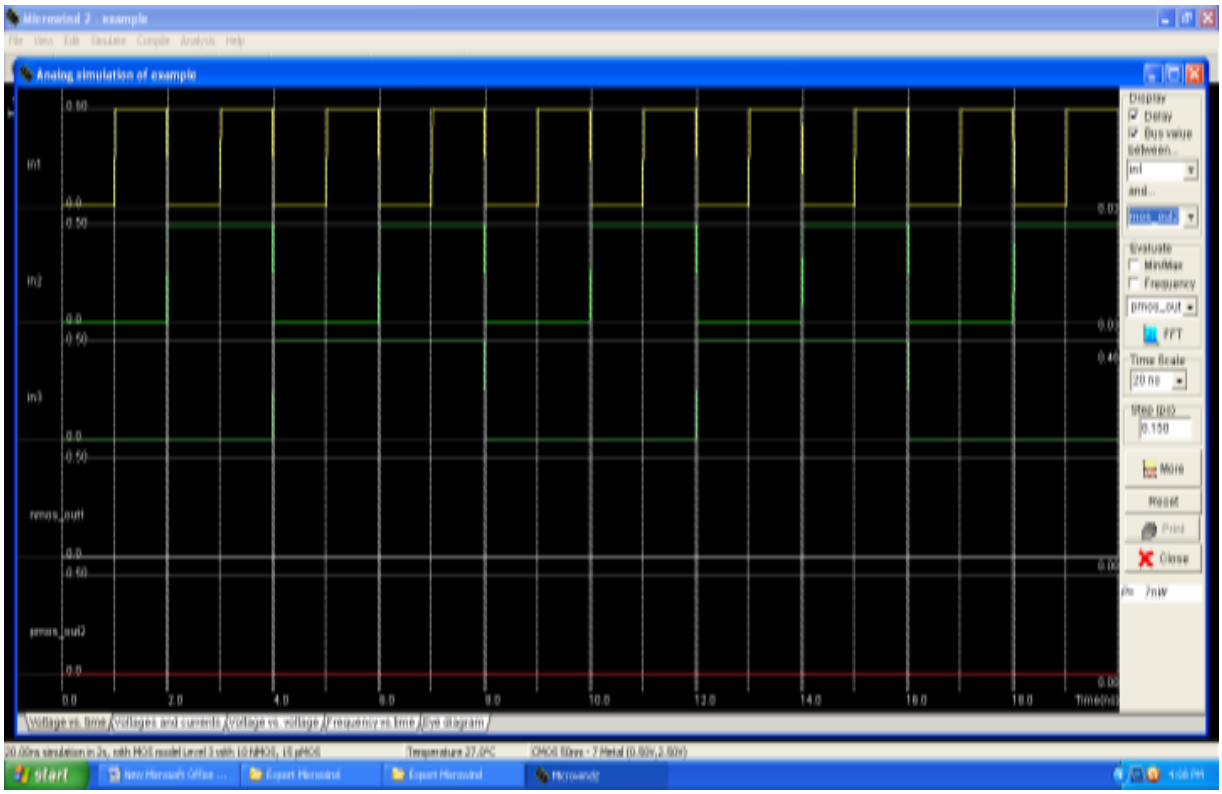




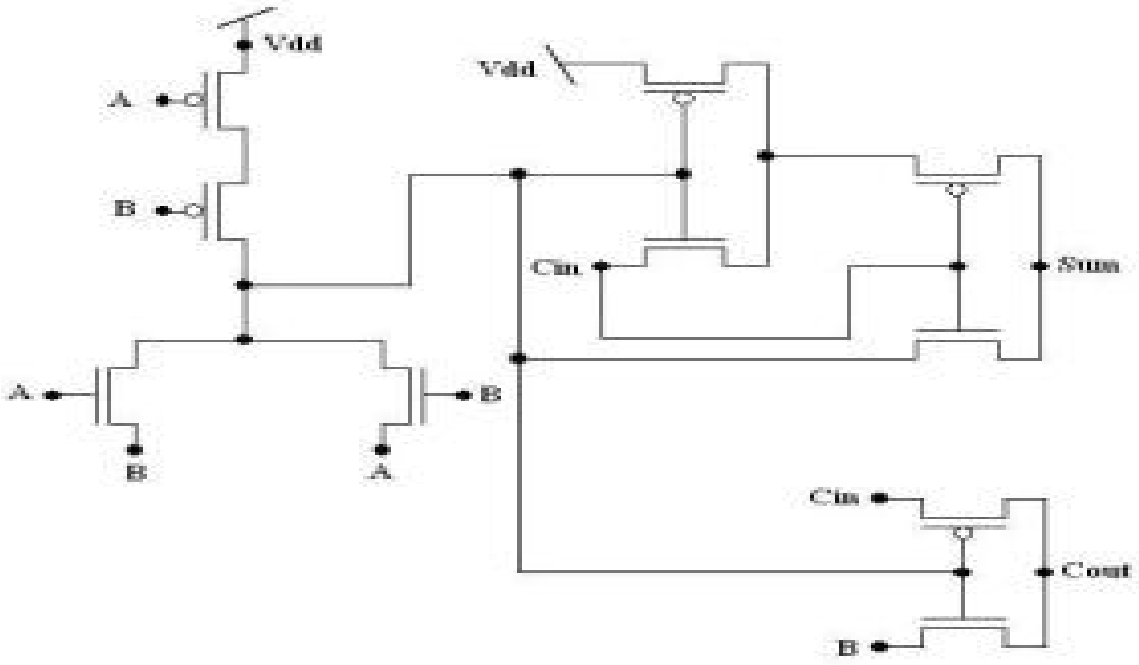
10T final Full Adder:-

Now using these GDI based XOR and XNOR gates two different GDI based full adder architecture were designed [Fig. E].

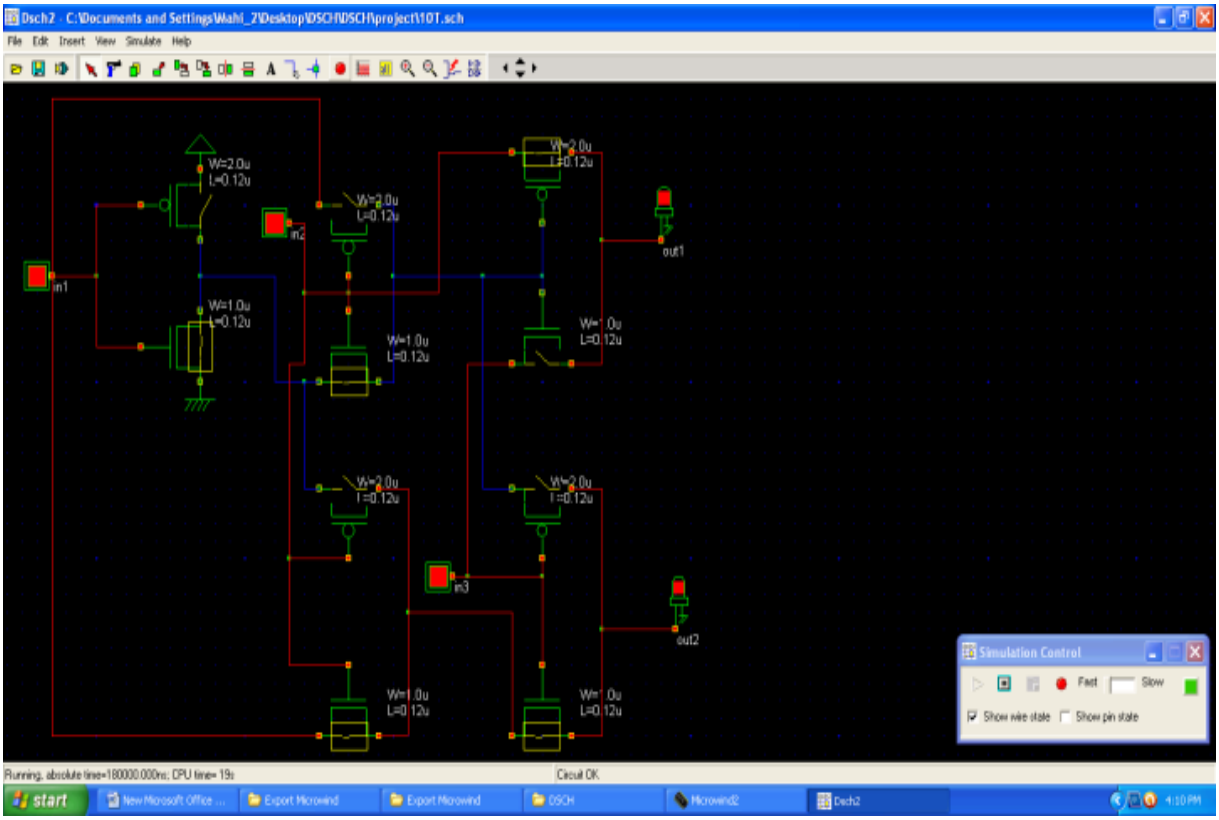
Circuit Operation The circuit operation of GDI Based Full Adders is exactly the same as that of previous SERF module. Sum bit is obtained from the output of the second stage of XOR, XNOR circuit while Carry bit (C_{ourt}) is calculated by multiplexing B and C_{in} controlled by (A XNOR B).

Advantage**:** These features give the GDI cell two extra input pins to use which makes it flexible than usual CMOS design. It is also a genius design which is very power efficient without huge amount of transistor count.

F. 10T Full Adder



DSCH DIAGRAME



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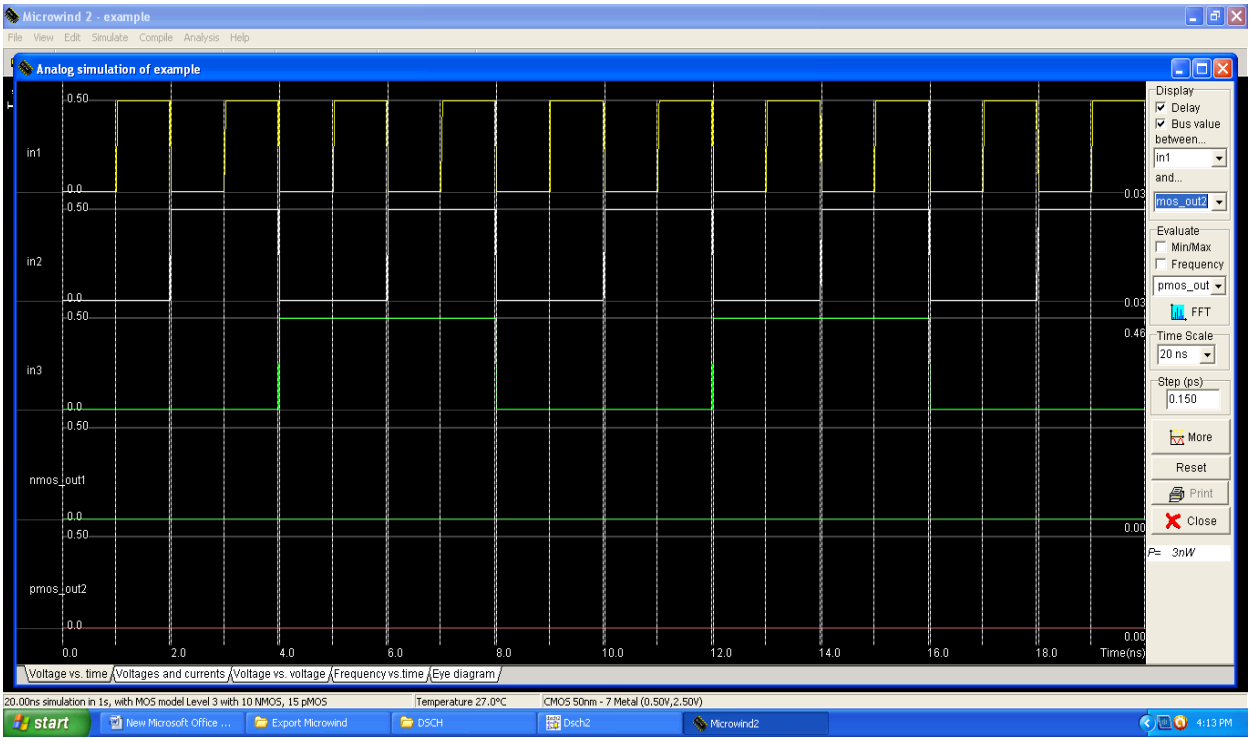

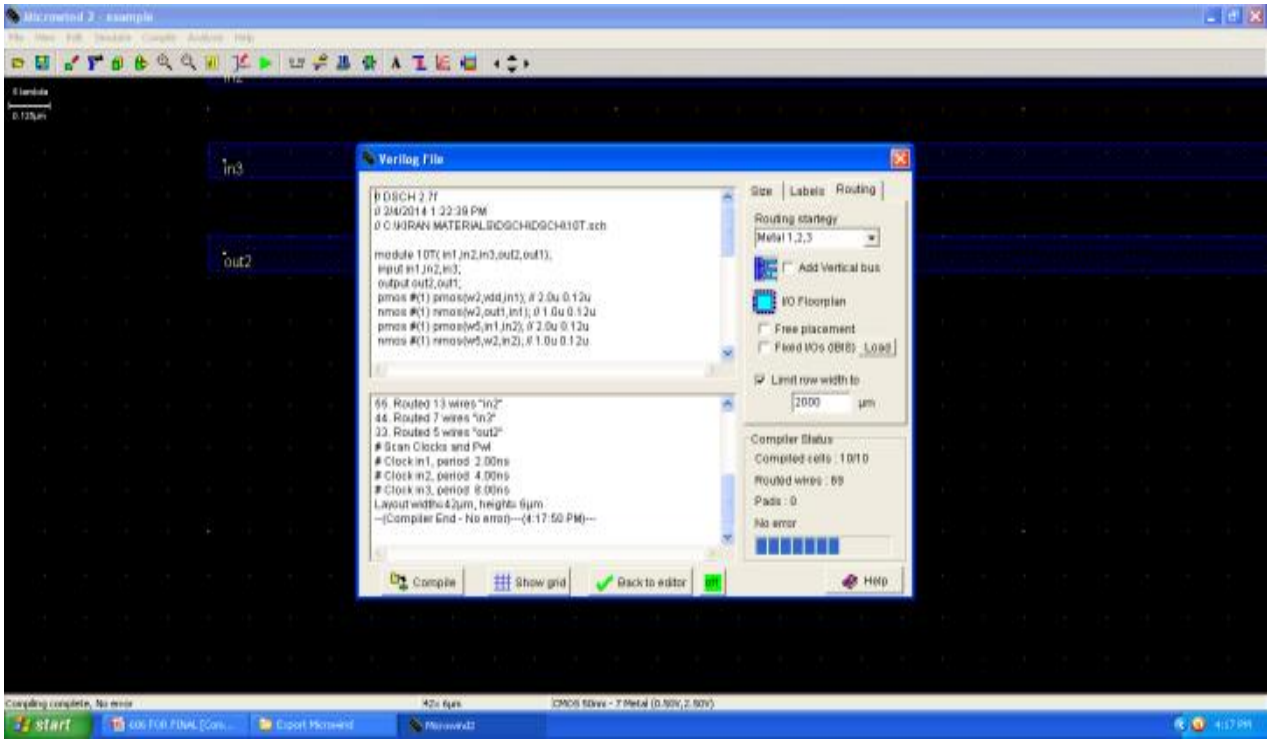

10T Full Adder:-

Now using these GDI based XOR and XNOR gates two different GDI based full adder architecture were designed [Fig. F] it is same as the 10T final full Adder .But here varying out put of power and area, here power consuming is 3nW ,and area (42*6)µm.

Circuit Operation: The circuit operation of GDI Based Full Adders is exactly the same as that of previous SERF module. Sum bit is obtained from the output of the second stage of XOR, XNOR circuit while Carry bit (C_{ourt}) is calculated by multiplexing B and C_{in} controlled by (A XNOR B).

Advantage: These features give the GDI cell two extra input pins to use which makes it flexible than usual CMOS design. It is also a genius design which is very power efficient without huge amount of transistor count.

III. IMPLEMENTATION RESULTS

3.1 Performance comparison of full adders

All the simulations were setup so as to drive the adder inputs through buffers and have the adder outputs drive buffers. The table reports the average power consumption when executing the set of all possible input combinations to the adders.

It can be seen that full adder

Name of the adder	Area(Microm^2)	Power(µW
CMOS FULL ADDER	(116*6)µm	0.032µW
MIRROR ADDER	(116*6)µm	0.033µW
TG ADDER	(83*6)µm	0.014µW
FULL ADDER 14T	(59*6)µm	4nW
10T FINAL FULL ADDER	(42*6)µm	7nW
10T FULL ADDER	(42*6)µm	3nW

14T provides the best PDP amongst all the adders when simulated stand alone. The full adder function characterized using the 10T full Adder methodology provide the lowest delay and after that TG adder and mirror adder. With respect to the choice of logic function to implement, the full adder was observed to perform the best when implemented using the *PROPAGATE* and *GENERATE* signals. This can be attributed to the fact that this function allows for smaller number of transistors stacked in series and shows the lowest capacitance at the output node. This shows that the capacitance at the output node forms the most critical component of the adder speed irrespective of the number of stages of circuits before getting the SUM and CARRY outputs

Also, with the increase in TOXE (gate oxide thickness) from 0.7 nm to 1.6 nm (this complicates the process), the large oxide thickness of the high-V_t, can reduce the gate capacitance which is beneficial for the reduction of sub threshold leakage power. Ultimately, the effective variation of MOSFET drains current, is therefore, determined by the variation of the dominant parameter. Here, carrier mobility with a large variation of **0.03 to 0.08 m^2/V-s** acts as a dominant parameter, hence drain current increases.

IV. CONCLUSION

The full adders such as Static CMOS Full Adder, Mirror, TG adders, Full Adder 14T, 10T final Full Adder , 10T Full adder .Sum and carry have been implemented by using Micro wind 3.1 CAD tool, among the all full adders, Full Adder 14T works very efficiently in the case of power consumption, performance and PDP. if we observe the geometric area, Mirror TG adder Full Adder 14T are better compared with other adders.

The observations that are made from the results of PVT variations on the performance of reduced swing domino logic circuits are given below. When process variations increase from VTHO=0.3 V, TOXE=0.7 nm, and UO=0.030 m^2/V-s to VTHO=0.4 V, TOXE=1.6 nm, and UO=0.08 m^2/V-s, power dissipation increases, I_{ON} increases, and I_{OFF} decreases. It is observed that when temperature increases from -13°C to 107°C, power dissipation increases, I_{ON} decreases, and I_{OFF} increases. The results show that with the increase of V_{DD} from 0.7 V to 0.8 V, the power dissipation, I_{ON}, I_{OFF} increase.

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